

<b>Notice of Allowability</b>	Application No.	Applicant(s)	
	09/828,283	MOBLEY, KENNETH J.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 10/21/5, notice of withdrawal.
2. ☒ The allowed claim(s) is/are 1-3, 5-7, 10, 25, 26, 11-13, 16-17, 20, 28, and 30 (renumbered to 1-17).
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All    b) ☐ Some\*    c) ☐ None    of the:
  1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☒ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
  - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
    - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
  - (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date 11/14/05.

**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

- |   |   |
|---|---|
| <ol style="list-style-type: none"> <li>1. <input type="checkbox"/> Notice of References Cited (PTO-892)</li> <li>2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</li> <li>3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),<br/>Paper No./Mail Date _____</li> <li>4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit<br/>of Biological Material</li> </ol> | <ol style="list-style-type: none"> <li>5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)</li> <li>6. <input type="checkbox"/> Interview Summary (PTO-413),<br/>Paper No./Mail Date _____</li> <li>7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment</li> <li>8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance</li> <li>9. <input checked="" type="checkbox"/> Other <u>New Fig. 9.</u></li> </ol> |
|---|---|

*HL*

### **Detailed Action**

1. Claims 1-3, 5-7, 10, 25, 26, 11-13, 16-17, 20, 28, and 30 are presented for examination. This office action is in response to the notice of withdrawal on 10/21/05.
2. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.
3. The status of the related U.S. applications must be updated accordingly (e.g., U.S. Patent Application Serial No. ####,### filled Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ####,###, filed on December 01, 1990, now abandoned; ...etc.) in the Related Applications section and in any other corresponding area in the specification, if any. Appropriate correction is required.

### **EXAMINER'S AMENDMENT**

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.
5. Authorization for this examiner's amendment was given in a telephone interview with George B.F. Yee, Attorney for Applicants (Reg. No. 37,478) November 7, 2005 in order to clarify 112 1st paragraph issue and place the claims in condition for allowance.

6. Application has been amended as follows:

In the specification:

Replace the two paragraphs beginning on page 3, line 24 of the specification as originally filed with the following three paragraphs:

Figure 7 is a schematic illustration of a pseudo-static memory architecture according to a third aspect of the present invention; [[and]]

Figure 8 is a timing diagram showing parallel read and refresh operations according to a sixth embodiment of the present invention[[.]]; and

Figure 9 illustrates the row addresses stored in each sub-array according to an addressing example.

Insert the following paragraph after line 22 on page 9:

Figure 9 illustrates the row addresses stored in each of the first, second, third, and fourth sub-arrays according to the above addressing example. The figure 9 shows an expansion of the row addresses in each sub-array per the addressing example. Thus, the figure shows an

expansion of addresses of the form XXX00XXXXXXX stored in the first sub-array. Likewise, the figure shows an expansion of addresses of the form XXX01XXXXXXX stored in the second sub-array. Similarly, the figure shows an expansion of addresses of the form XXX10XXXXXXX stored in the third sub-array. Finally, the figure the figure shows an expansion of addresses of the form XXX11XXXXXXX stored in the fourth sub-array.

Add Fig. 9 in the drawing (see attachment)

In the claim:

Cancel claims 27, 29, and 31.

Amend Claim 1, 11, 28, and 30

1. (Currently amended) A memory device having plural DRAM sub-arrays, each with plural array rows, comprising:  
an address decoder for decoding an address of a *memory* access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request; and  
refresh circuitry, responsive to the indication of the address decoder, to refresh at least one array row of at

least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory request, wherein logically adjacent rows are placed in different sub-arrays,

wherein a first row is in a first sub-array and a second row is in a second sub-array, the second row being one logical row from the first row, and a third row is in the first sub-array and a fourth row is in the second sub-array, the fourth row being one logical row from the third row, wherein the first row is not logically adjacent to the third row.

11. (Currently amended) A method of refreshing a memory device having a plural DRAM sub-arrays, each with plural array rows, the method comprising:

(a) placing logically adjacent rows in different sub-arrays, wherein a first row is in a first sub-array and a second row is in a second sub-array, the second row being one logical row from the first row, and a third row is in the first sub-array and a fourth row is in the second sub-array, the fourth row being one logical row from the third row, wherein the first row is not logically adjacent to the third row;

- (b) decoding an address of a memory request;
  - (c) indicating which of the plural DRAM sub-arrays are referenced by the memory access request;
  - (d) refreshing, in response to the indicating step, at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request; and
  - (e) executing the memory address request,
- wherein steps (d) and (e) are performed contemporaneously.

28. (Currently amended) A memory device having plural DRAM sub-arrays, each with plural array rows, comprising:

an address decoder for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request; and

refresh circuitry, responsive to the indication of the address decoder, to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory request, wherein logically adjacent rows are placed in different sub-arrays, and the logically adjacent rows in different sub-arrays comprise rows other than the last and first rows of consecutive sub-arrays,

wherein each sub-array includes rows that are not logically adjacent.

30, (Currently amended) A method of refreshing a memory device having a plural DRAM sub-arrays, each with plural array rows, the method comprising:

(a) placing logically adjacent rows in different sub-arrays, and the logically adjacent rows in different sub-arrays comprise rows other than the last and first rows of consecutive sub-arrays, wherein each sub-array includes rows that are not logically adjacent;

(b) decoding an address of a memory request;

(c) indicating which of the plural DRAM sub-arrays are referenced by the memory access request;

(d) refreshing, in response to the indicating step, at least one array row of at least one of the I plural DRAM sub-arrays not referenced by the memory access request; and

(e) executing the memory address request,  
wherein steps (d) and (e) are performed contemporaneously.

**REASONS for ALLOWANCE**

7. The following is an Examiner's statement of reasons for the indication of allowable subject matter: renumbered claims 1-17 are allowable over the prior art of record because an update of a search previously made does not detect the combined claimed elements as set forth in the claims 1-17. Specifically, claims are allowable over the prior art of record because none of the prior art of record teaches or fairly suggests hidden refresh method and apparatus for logical DRAM sub-arrays as described in the specification and together with combination of other claimed element as set forth in the claims. Also the reasons for allowance of the claims over the prior art of record is believed to be clear from the prosecution records taken as a whole. Therefore, claims 1-17 are allowable over the prior art of records.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably **accompany** the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons For Allowance."

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should

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be directed to the TC 2100 whose telephone number is (571) 272-2100.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

11. **Any response to this action should be mailed to:**

Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**or faxed to TC-2100:**  
(703) 872-9306

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

H Kim  
Primary Patent Examiner  
November 14, 2005



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Add Fig. 9 in the drawing (see attachment)

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refresh circuitry, responsive to the indication of the address decoder, to refresh at least one array row of at

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wherein a first row is in a first sub-array and a second row is in a second sub-array, the second row being one logical row from the first row, and a third row is in the first sub-array and a fourth row is in the second sub-array, the fourth row being one logical row from the third row, wherein the first row is not logically adjacent to the third row.

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~~11~~. (Currently amended) A method of refreshing a memory device having a plural DRAM sub-arrays, each with plural array rows, the method comprising:

(a) placing logically adjacent rows in different sub-arrays, wherein a first row is in a first sub-array and a second row is in a second sub-array, the second row being one logical row from the first row, and a third row is in the first sub-array and a fourth row is in the second sub-array, the fourth row being one logical row from the third row, wherein the first row is not logically adjacent to the third row;

- (b) decoding an address of a memory request;
  - (c) indicating which of the plural DRAM sub-arrays are referenced by the memory access request;
  - (d) refreshing, in response to the indicating step, at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request; and
  - (e) executing the memory address request,
- wherein steps (d) and (e) are performed contemporaneously.

<sup>16</sup>  
~~28~~. (Currently amended) A memory device having plural DRAM sub-arrays, each with plural array rows, comprising:

- an address decoder for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request; and
- refresh circuitry, responsive to the indication of the address decoder, to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory request, wherein logically adjacent rows are placed in different sub-arrays, and the logically adjacent rows in different sub-arrays comprise rows other than the last and first rows of consecutive sub-arrays,

wherein each sub-array includes rows that are not logically adjacent.

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~~20~~, (Currently amended) A method of refreshing a memory device having a plural DRAM sub-arrays, each with plural array rows, the method comprising:

(a) placing logically adjacent rows in different sub-arrays, and the logically adjacent rows in different sub-arrays comprise rows other than the last and first rows of consecutive sub-arrays, wherein each sub-array includes rows that are not logically adjacent;

(b) decoding an address of a memory request;

(e) indicating which of the plural DRAM sub-arrays are referenced by the memory access request;

(d) refreshing, in response to the indicating step, at least one array row of at least one of the I plural DRAM sub-arrays not referenced by the memory access request; and

(e) executing the memory address request,  
wherein steps (d) and (e) are performed contemporaneously.

**REASONS for ALLOWANCE**

Attachment

FACSIMILE

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<u>1<sup>st</sup> sub-array</u>	<u>2<sup>nd</sup> sub-array</u>	<u>3<sup>rd</sup> sub-array</u>	<u>4<sup>th</sup> sub-array</u>
000000000000	000010000000	000100000000	000110000000
000000000001	000010000001	000100000001	000110000001
000000000010	000010000010	000100000010	000110000010
⋮	⋮	⋮	⋮
000001111111	000011111111	000101111111	000111111111
001000000000	001010000000	001100000000	001110000000
001000000001	001010000001	001100000001	001110000001
001000000010	001010000010	001100000010	001110000010
⋮	⋮	⋮	⋮
001001111111	001011111111	001101111111	001111111111
010000000000	010010000000	010100000000	010110000000
010000000001	010010000001	010100000001	010110000001
010000000010	010010000010	010100000010	010110000010
⋮	⋮	⋮	⋮
010001111111	010011111111	010101111111	010111111111
011000000000	011010000000	011100000000	011110000000
011000000001	011010000001	011100000001	011110000001
011000000010	011010000010	011100000010	011110000010
⋮	⋮	⋮	⋮
011001111111	011011111111	011101111111	011111111111
100000000000	100010000000	100100000000	100110000000
100000000001	100010000001	100100000001	100110000001
100000000010	100010000010	100100000010	100110000010
⋮	⋮	⋮	⋮
100001111111	100011111111	100101111111	100111111111
101000000000	101010000000	101100000000	101110000000
101000000001	101010000001	101100000001	101110000001
101000000010	101010000010	101100000010	101110000010
⋮	⋮	⋮	⋮
101001111111	101011111111	101101111111	101111111111
110000000000	110010000000	110100000000	110110000000
110000000001	110010000001	110100000001	110110000001
110000000010	110010000010	110100000010	110110000010
⋮	⋮	⋮	⋮
110001111111	110011111111	110101111111	110111111111
111000000000	111010000000	111100000000	111110000000
111000000001	111010000001	111100000001	111110000001
111000000010	111010000010	111100000010	111110000010
⋮	⋮	⋮	⋮
111001111111	111011111111	111101111111	111111111111

FIG. 9

" Attachment # FACSIMILE

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<u>1<sup>st</sup> sub-array</u>	<u>2<sup>nd</sup> sub-array</u>	<u>3<sup>rd</sup> sub-array</u>	<u>4<sup>th</sup> sub-array</u>
000000000000	000010000000	000100000000	000110000000
000000000001	000010000001	000100000001	000110000001
000000000010	000010000010	000100000010	000110000010
⋮	⋮	⋮	⋮
000001111111	000011111111	000101111111	000111111111
001000000000	001010000000	001100000000	001110000000
001000000001	001010000001	001100000001	001110000001
001000000010	001010000010	001100000010	001110000010
⋮	⋮	⋮	⋮
001001111111	001011111111	001101111111	001111111111
010000000000	010010000000	010100000000	010110000000
010000000001	010010000001	010100000001	010110000001
010000000010	010010000010	010100000010	010110000010
⋮	⋮	⋮	⋮
010001111111	010011111111	010101111111	010111111111
011000000000	011010000000	011100000000	011110000000
011000000001	011010000001	011100000001	011110000001
011000000010	011010000010	011100000010	011110000010
⋮	⋮	⋮	⋮
011001111111	011011111111	011101111111	011111111111
100000000000	100010000000	100100000000	100110000000
100000000001	100010000001	100100000001	100110000001
100000000010	100010000010	100100000010	100110000010
⋮	⋮	⋮	⋮
100001111111	100011111111	100101111111	100111111111
101000000000	101010000000	101100000000	101110000000
101000000001	101010000001	101100000001	101110000001
101000000010	101010000010	101100000010	101110000010
⋮	⋮	⋮	⋮
101001111111	101011111111	101101111111	101111111111
110000000000	110010000000	110100000000	110110000000
110000000001	110010000001	110100000001	110110000001
110000000010	110010000010	110100000010	110110000010
⋮	⋮	⋮	⋮
110001111111	110011111111	110101111111	110111111111
111000000000	111010000000	111100000000	111110000000
111000000001	111010000001	111100000001	111110000001
111000000010	111010000010	111100000010	111110000010
⋮	⋮	⋮	⋮
111001111111	111011111111	111101111111	111111111111

FIG. 9